

WHAT IS CLAIMED IS:

1 ~~1~~ 1 A substrate comprising:

2 ~~2~~ pads which are provided on the surface of said
3 substrate; and

4 surface layers which are kept to the ground potential
5 and cover the surface of said substrate except said pads and
6 their peripheral.

1 2. The substrate as claimed in claim 1, wherein said surface
2 layers includes a top main surface and a bottom main surface.

1 3. The substrate as claimed in claim 2, further comprising:
2 a conductive element which electronically connects said
3 top main surface and said bottom main surface.

1 ~~2~~ 4. The substrate as claimed in claim ~~2~~, further comprising:
2 vias which electronically connects said top main surface
3 and said bottom main surface.

1 ~~3~~ 5. The substrate as claimed in claim ~~4~~, wherein said vias
2 are provided on the side portion of said substrate.

1 ~~4~~ 6. The substrate as claimed in claim ~~5~~, wherein said surface
2 layers further includes a side layer which electronically
3 connects said top main surface and said bottom main surface.

1 ~~5~~ 7. The substrate as claimed in claim 1, wherein said surface

2 layers includes six surface layers.

1 ~~6~~ 8. The substrate as claimed in claim 1, further comprising
2 a signal layer which is provided between said top main surface
3 and said bottom main surface, and has a pattern which is
4 connected to at least one of said pads.

1 ~~7~~ 9. The substrate as claimed in claim 1, wherein an interval
2 between said pad and said surface layer is defined to prevent
3 said pad from short-circuiting.

1 10. A substrate comprising:

2 a part of circuit which is provided on the surface of said
3 substrate; and

4 a surface layers which are kept to the ground potential
5 and cover the surface of said substrate except said part of
6 circuit and its peripheral.

1 11. The substrate as claimed in claim 1, wherein said surface
2 layers includes a top main surface and a bottom main surface.

1 12. The substrate as claimed in claim 2, further comprising:
2 a conductive element which electronically connects said
3 top main surface and said bottom main surface.

1 13. The substrate as claimed in claim 2, further comprising:
2 vias which electronically connects said top main surface
3 and said bottom main surface.

1 14. The substrate as claimed in claim 4, wherein said vias
2 are provided on the side portion of said substrate.

1 15. The substrate as claimed in claim 2, wherein said surface
2 layers further includes a side layer which electronically
3 connects said top main surface and said bottom main surface.

1 16. The substrate as claimed in claim 1, wherein said surface
2 layers includes six surface layers.

1 17. The substrate as claimed in claim 1, further comprising
2 a signal layer which is provided between said top main surface
3 and said bottom main surface, and has a pattern which is
4 connected to said part of circuit.

1 18. The substrate as claimed in claim 1, wherein an interval
2 between said part of circuit and said surface layer is defined
3 to prevent said part of circuit form short-circuiting.